UNITED STATES PATENT AND TRADEMARK OFFICE

# CERTIFICATE OF CORRECTION

PATENT NO. : 6,771,553 B2
APPLICATION NO. : 10/056935
DATED : August 3, 2004
INVENTOR(S) : Timothy B. Cowles, Brian M. Shirley and Greg A. Blodgett



It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

| Column, Line | Reads | Should Read |
|---|---|---|
| Column 2, Line 49 | "spurious command" | --spurious commands-- |
| Column 6, Lines 1-6 | "After the input buffers **110** are enabled by a high IBENCLK signal, the IBENCMD signal transitions high to switch the input buffers **110** to a low impedance state and to turn OFF the transistors **130-136** so they do not affect the at time $T_0$ and registered at time $T_1$ by the rising edge of the external clock CLK signal." | --After the input buffers **110** are enabled by a high IBENCLK signal, the IBENCMD signal transitions high to switch the input buffers **110** to a low impendance state and to turn OFF the transistors **130-136** so they do not affect the operation of the power saving circuit **100**. When the input buffers **110** are switched to a high impedance state by a low IBENCLK signal, the transistors **130-136** are turned ON to bias high respective internal command signal lines to which they are coupled.<br>The internal command signals IRAS*, ICAS*, IWE*, and ICS*, as well as other internal command signals from the input buffers **110**, are applied to a command decoder unit **140**. The command decoder unit **140** generates a plurality of memory commands, including an auto-refresh command |

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| Column, Line | Reads | Should Read |
|---|---|---|
| Column 6, Lines 1-6 (cont'd) | | AREF, from various combinations of the command signals applied to its inputs. As explained above, the AREF command is asserted responsive to decoding IRAS*, ICAS*, and ICS* active low and IWE* inactive high.<br>The auto-refresh command AREF is applied to a refresh decoder **150** along with the internal clock ICLK signal and the internal clock enable ICKE signal. Based on the state of the ICKE signal, the refresh decoder **150** determines if the AREF command is for an auto-refresh or if is for a self-refresh. If ICKE is high, the AREF command is interpreted as an auto-refresh command, in which case the refresh decoder **150** passes the AREF command to an output terminal as an AREF' command. If ICKE is low, the AREF command is interpreted as a self-refresh command, in which |

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| Column, Line | Reads | Should Read |
|---|---|---|
| Column 6, Lines 1-6 (cont'd) | | case the refresh decoder **150** generates a SREF command. The refresh decoder **150** command will continue to generate the SREF command until the ICKE signal transitions high.<br>The AREF command is also applied to a timer **154,** which generates a $T_{OUT}$ pulse after a predetermined period. The $T_{OUT}$ pulse causes the refresh decoder **150** to terminate the AREF' command, thereby terminating the auto-refresh cycle.<br>All of the input buffers **110, 120, 124** as well as the transistors **130-136,** the inverter **138,** the command decoder unit **140,** the refresh decoder **150** and the timer **154,** are shown in FIG. **2** as being located in the command decoder **4.** However, as previously mentioned, these components could alternatively be located elsewhere in the SDRAM **2** or in other memory devices.<br>The operation of the |

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| Column, Line | Reads | Should Read |
|---|---|---|
| Column 6, Lines 1-6 (cont'd) | | power saving circuit **100** will now be explained with reference to the timing diagram of FIG. **3**. The combination of control signals ("CMD") that constitute an auto-refresh AREF command are applied to the SDRAM **2** at time $T_0$ and registered at time $T_1$ by the rising edge of the external clock CLK signal.-- |
| Column 7, Lines 14-66 | "The operation of the power saving circuit **200** is substantially the same as the power saving circuit **100**. Specifically, in response to registering an AREF command, the IBENCMD, IBENADD and IBENCLK signals transition low to disable the input buffers **102, 110** and the internal clock buffer **230.** As a result, neither the input buffers **102, 110** nor circuitry (not shown) downstream from the internal clock buffer **230** consume power during the auto-refresh cycle initiated in response to the operation of the power saving circuit **100**. When the input buffers **110** are switched to | --The operation of the power saving circuit **200** is substantially the same as the power saving circuit **100**. Specifically, in response to registering an AREF command, the IBENCMD, IBENADD and IBENCLK signals transition low to disable the input buffers **102, 110** and the internal clock buffer **230.** As a result, neither the input buffers **102, 110** nor circuitry (not shown) downstream from the internal clock buffer **230** consume power during the auto-refresh cycle initiated in response to the AREF |

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| Column, Line | Reads | Should Read |
|---|---|---|
| Column 7, Lines 14-66 (cont'd) | a high impedance state by a low IBENCLK signal, the transistors **130-136** are turned ON to bias high respective internal command signal lines to which they are coupled.<br>The internal command signals IRAS*, ICAS*, IWE*, and ICS*, as well as other internal command signals from the input buffers **110,** are applied to a command decoder unit **140**. The command decoder unit **140** generates a plurality of memory commands, including an auto-refresh command AREF, from various combinations of the command signals applied to its inputs. As explained above, the AREF command is asserted responsive to decoding IRAS*, ICAS*, and ICS* active low and IWE* inactive high.<br>The auto-refresh command AREF is applied to a refresh decoder **150** along with the internal clock ICLK signal and the internal clock enable ICKE signal. Based on the state of the ICKE signal, the refresh decoder **150** determines if the AREF command is for an auto- | command.-- |

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| Column, Line | Reads | Should Read |
|---|---|---|
| Column 7, Lines 14-66 (cont'd) | refresh or if it is for a self-refresh. If ICKE is high, the AREF command is interpreted as an auto-refresh command, in which case the refresh decoder **150** passes the AREF command to an output terminal as an AREF' command. If ICKE is low, the AREF command is interpreted as a self-refresh command, in which case the refresh decoder **150** generates a SREF command. The refresh decoder **150** command will continue to generate the SREF command until the ICKE signal transitions high.<br>The AREF command is also applied to a timer **154**, which generates a $T_{OUT}$ pulse after a predetermined period. The $T_{OUT}$ pulse causes the refresh decoder **150** to terminate the AREF' command, thereby terminating the auto-refresh cycle.<br>All of the input buffers **110, 120, 124** as well as the transistors **130-136**, the inverter **138** the command decoder unit **140,** the refresh decoder **150** and the timer **154**, are shown in | |

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| Column, Line | Reads | Should Read |
|---|---|---|
| Column 7, Lines 14-66 (cont'd) | FIG. **2** as being located in the command decoder **4**. However, as previously mentioned, these components could alternatively be located elsewhere in the SDRAM **2** or in other memory devices. The operation of the power saving circuit **100** will now be explained with reference to the timing diagram of FIG. **3**. The combination of control signals ("CMD") that constitute an auto-refresh AREF command are applied to the SDRAM **2** AREF command." | |
| Column 8, Line 41 | "("0" for full AREF period)" | --"0" (for full AREF period)-- |
| Column 8, Line 54 | "when the AREF command" | --when the AREF command is asserted-- |
| Column 8, Lines 56 and 62 | "to end of the" | --to end the-- |
| Column 10, Line 23 | "operable to removing" | --operable to remove-- |
| Column 11, Line 54 | "and a detecting" | --and detecting a-- |
| Column 12, Line 37 | "transition terminate" | --transition to terminate-- |
| Column 13, Lines 3 and 5 | "and decoder" | --and decode-- |
| Column 13, Line 17 | "coupled thorough" | --coupled through-- |
| Column 14, Line 64 | "coupled thorough" | --coupled through-- |

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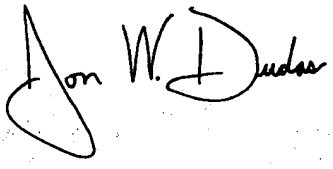
| Column, Line | Reads | Should Read |
|---|---|---|
| Column 16, Lines 43 and 46 | "decoder" | --decode-- |
| Column 16, Line 59 | "and coupled thorough" | --and coupled through-- |
| Column 17, Line 8 | "to removing" | --to remove-- |
| Column 18, Lines 3 and 6 | "decoder" | --decode-- |
| Column 18, Line 21 | "coupled thorough" | --coupled through-- |
| Column 19, Line 22 | "claim **63**" | --claim **62**-- |
| Column 22, Line 4 | "claim **89**" | --claim **88**-- |

Signed and Sealed this

Tenth Day of October, 2006



JON W. DUDAS
*Director of the United States Patent and Trademark Office*